Average model of a synchronous half-bridge DC/DC converter considering losses and dynamics

Michael Winter[1] Sascha Moser[1] Stefan Schoenewolf[1] Julian Taube[1]
Hans-Georg Herzog[1]

[1]Institute for Energy Conversion Technology, Technische Universitaet Muenchen, Germany,
michael.winter@tum.de

Abstract

Nowadays, power electronic systems play a major role in almost every large system. Due to the high switching frequencies, the simulation of these devices is computationally very expensive and not suitable for system simulation. Average models of these power electronic systems are needed to simulate the basic terminal characteristics of these devices without the need to simulate every switching operation. This paper describes a Modelica implementation of a synchronous half-bridge converter for the use in an automotive power net simulation as well as in real-time environments. The model takes into account the losses in the semiconductors as well as the dynamic behavior of the converter. For the parametrization of the model, only the switching frequency and some values from the datasheets of the used components are required. To validate the proposed model, an equivalent SPICE model is developed, serving as a reference model. The dynamic behavior of the two models is compared using step responses of the load current. The relative deviation of the model's output voltage compared to the SPICE simulation is less than 2 %. Furthermore, also the energetic behavior was investigated, and it is shown that the proposed model provides good results for a wide operating area.

Keywords: power electronics, average model, DC/DC converter, losses, acausal modeling

1 Introduction

DC/DC converters are used to convert a DC input voltage into a DC output voltage with a higher, lower or inverted value. In the automotive power net, such power electronic circuits are used extensively. Almost every electronic control unit (ECU) has a DC/DC converter close to its terminals to the power net side in order to compensate voltage fluctuations and to supply the electronics with a constant voltage. In addition, DC/DC converters are used to control DC motors, to couple the 48V level with the 12V power net or to stabilize the 12V power net with an additional energy storage (Ruf et al., 2012).

In today's product development processes, simulation is a very important step. With the help of simulation, development cycles can be shortened and costs can be reduced. When simulating power electronic systems, several engineering challenges have to be solved. During the development phase, the DC/DC converter is usually simulated with SPICE (Simulation Program with Integrated Circuit Emphasis) or a similar software. The behavior of the converter is primarily determined by the power semiconductors and passive components. The passive components can be easily modeled in SPICE and the power semiconductor manufacturers provide more or less accurate models for their products. The major advantage of a SPICE simulation is that the dynamic behavior and all loss mechanisms in a power electronic system are taken into account. The simulation is computationally quite intensive, however, the long computation times are not a big issue in this development phase as only short periods of time are considered and usually only one or a small number of converters are simulated simultaneously.

For system simulation however, these models are not suitable for two reasons. On the one hand, in contrast to Modelica, SPICE does not meet the requirements of multi-domain simulation. There are already approaches to translate SPICE models into the Modelica language (Majetta et al., 2011) and it also has been shown that Modelica is in principle suitable for simulation of power electronics (Glaser et al., 1995). None of these approaches solves the second challenge, that the calculation of the switching operations would slow down the system simulation, so it would be practically impossible to carry out longer simulations. Another approach is to build behavioral or loss models. The various loss mechanisms in power electronic converters are well understood and can be described by algebraic equations

(Giuliani et al., 2011; Gragger, 2011). However, this type of modeling neglects the dynamic behavior of the passive components.

2 Objectives and Approach

This paper describes an average model of a synchronous half-bridge converter in continuous conduction mode, considering the converter's dynamics and losses. In future work, the model will be used both in the Modelica-based automotive power net simulation environment (Ruf et al., 2013) as well as in real-time operation in an automotive power net test bench (Kohler et al., 2010). For parametrization of the model, only the switching frequency and the datasheet parameters of the power semiconductors, the inductance, and the capacitors are needed. The model is validated by means of an equivalent SPICE model.

3 The Synchronous Half-Bridge Converter

The converter model presented in this work is based on a synchronous half-bridge converter as shown in Figure 1. The fundamentals presented in this chapter are well known and documented in literature (Kazimierczuk, 2008; Erickson and Maksimović, 2001), as well as in application sheets provided by the semiconductor manufacturers (Vishay, 2002). The converter consists of a high-side switch S, a low-side switch $\bar{S}$, an inductor L, and capacitors at the input and output. Basically it is a standard buck or boost converter topology with the freewheeling diode replaced by a second switch in order to reduce conduction losses. Furthermore, the topology becomes bidirectional by this change where the voltage v_1 is always higher than the voltage v_2. The direction of the energy flow can be controlled by the duty cycle D.

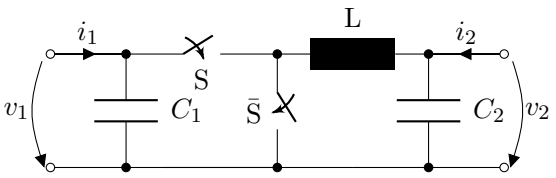

Figure 1. Topology of a synchronous half-bridge

3.1 General equations for the synchronous half-bridge

The two switches are controlled by complementary pulse width modulated signals with the switching frequency f_S. The duty cycle D relates in the following always to the high-side switch S and is defined as follows:

$$D = \frac{t_{on}}{T_S} = \frac{t_{on}}{t_{on} + t_{off}} = f_S \cdot t_{on} \tag{1}$$

The transfer equations for a loss-less half-bridge containing no storing elements such as inductors or capacitors are the same as for an ideal DC-transformer:

$$v_2 = D \cdot v_1 \tag{2}$$

$$i_2 \cdot D = -i_1 \tag{3}$$

In order to obtain a transformer considering the ohmic and the switching losses, equation (2) is replaced by a power balance equation that interrelates input power, output power and power dissipation:

$$P_1 + P_2 - P_L = 0 \tag{4}$$

The load dependent losses of the half-bridge are composed of the losses of the high-side and the low-side switch. In each switch, conduction losses occur and depending on the mode, also switching losses.

$$P_L = P_{L,S,cond} + P_{L,S,sw} + P_{L,\bar{S},cond} + P_{L,\bar{S},sw} \tag{5}$$

The load dependent loss mechanisms in the semiconductors are presented separately in the following two subsections. For switching losses, the turn-on and turn-off times of the power semiconductors have a major impact. In this work, the simplifying assumption is made that both switches are the same and the driver circuit has an ideal behavior, providing similar rise and fall times t_{rise} and t_{fall}. Thus, switching times are simply a function of the the total gate charge Q_g, the operating voltage of the gate-drive circuit U_{drive} and the sum of the gate driver's output resistance, the gate series resistance and the gate's input resistance, called $R_{g,total}$.

$$t_{rise} = t_{fall} = \frac{Q_g \cdot R_{g,total}}{U_{drive}} \tag{6}$$

In addition the continuous charging and discharging of the semiconductor's gates causes losses which have to be covered by the gate driver. These losses are a function of the total gate charge $Q_{g,total}$, the driving voltage V_{drive} and the switching frequency.

$$P_{L,Gate} = Q_{g,total} \cdot V_{drive} \cdot f_S \tag{7}$$

3.2 Loss equations for the synchronous half-bridge in buck mode

In buck mode the high-side switch is obligatory, so conduction and switching losses occur:

$$P_{L,S,cond} = R_{DS,on} \cdot i_2^2 \cdot D \tag{8}$$

$$P_{L,S,sw} = 0.5 \cdot v_1 \cdot (-i_2) \cdot (t_{fall} + t_{rise}) \cdot f_S \tag{9}$$

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The low-side switch does not have to switch the current but supports the loss reduction in the commutation path. For simplicity it is assumed that losses through the conducting diode during the dead times and the reverse recovery effect can be neglected, so here only conduction losses occur:

$$P_{L,\bar{S},cond} = R_{DS,on} \cdot i_2^2 \cdot (1-D) \tag{10}$$

$$P_{L,\bar{S},sw} = 0 \tag{11}$$

3.3 Loss equations for the synchronous half-bridge in boost mode

The low-side switch is the primary switch during boost mode operation, the losses are described by following equations:

$$P_{L,\bar{S},cond} = R_{DS,on} \cdot i_1^2 \cdot (1-D) \tag{12}$$

$$P_{L,\bar{S},sw} = 0.5 \cdot v_2 \cdot (-i_1) \cdot (t_{fall} + t_{rise}) \cdot f_S \tag{13}$$

The high-side switch is part of the commutation path, so there are only conduction losses:

$$P_{L,S,cond} = R_{DS,on} \cdot i_1^2 \cdot \frac{(1-D)}{D^2} \tag{14}$$

$$P_{L,S,sw} = 0 \tag{15}$$

4 Models

In this chapter, the proposed Modelica model of a synchronous half-bridge converter is presented. Then the equivalent model is implemented in SPICE and serves as a reference model in chapter 5.

4.1 Modelica implementation of the synchronous half-bridge converter

The implementation of the model of the proposed half-bridge converter is based on the averaged circuit model for a two-switch converter (Erickson and Maksimović, 2001). The model is obtained by taking the basic structure of the real converter including the inductance and capacitances. Then, the switches have to be replaced by an averaged switch model, as shown in Figure 2. The electrical connectors $p1$ and $n1$ provide the terminals for the high-voltage side, the connectors $p2$ and $n2$ for the low-voltage side, and the connectors p_a and n_a for the auxiliary power supply. The auxiliary power supply can optionally be charged with a constant power loss in order to take the power for the converter's control into account. The transfer function and the loss equations of the semiconductors of the synchronous half-bridge are implemented in a separate model named *AveragingHalfBridge*. This sub-model contains equations (3) - (7)

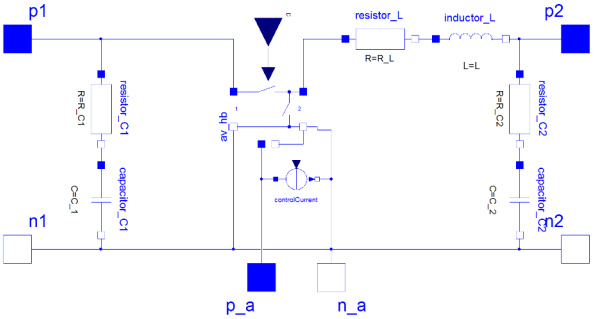

Figure 2. Model of the proposed synchronous half-bridge converter

and is able to swap between the two equation systems (8) - (11) for buck and (12) - (15) for boost mode, depending on the actual current direction. The *AveragingHalfBridge* is derived from the base class *Modelica.Electrical.Analog.Interfaces.TwoPort* of the *Modelica Standard Library* which also defines the directions of the currents and voltages of the equation system. The sub-model receives the actual duty cycle D of the half-bridge as a real input and is parametrized with the following values:

- The switching frequency f_S of the half-bridge.
- The on-resistance $R_{DS,on}$ and the total gate charge $Q_{g,total}$ of the MOSFET, both values can be taken from the MOSFET's datasheet.
- The operating voltage of the gate-drive circuit U_{drive} and total gate resistance $R_{g,total}$, determined by design and the MOSFET's and driver's parameters from the datasheet.

The dynamic behavior of the converter is determined by the input and output capacitors, the inductance and the respective series resistances of these components:

- The capacitance C_1 and the equivalent series resistance of the capacitor R_{C1} on the high-voltage side of the converter.
- The inductance L and the equivalent series resistance of the inductor R_L.
- The capacitance C_2 and the equivalent series resistance of the capacitor R_{C2} on the low-voltage side of the converter.

4.2 SPICE model as reference for validation

For the validation of the Modelica model, a SPICE model for comparative simulations is implemented which is shown in Figure 3. This model takes the switching behavior of the real converter into account. The passive components of the converter

like input and output capacitors and inductor are directly inserted from the SPICE library. These components are parametrized to the same component values as for the Modelica model in subsection 4.1, taking into account the ohmic resistance of the inductor and the equivalent series resistance of the capacitors. For the MOSFETs and antiparallel freewheeling diodes SPICE models provided by the semiconductor manufacturers are used. The gate drivers are modeled by time varying voltage sources. An additional resistor corresponds to the gate driver's output resistance and gate series resistance whereas the gate's input resistance is provided by the model of the MOSFET. Dead time as well as rise and fall times of the gate driver are set by the voltage shape of the voltage sources. As all parameters and submodels of the SPICE model are selected very close to physical realizations, this model is well suited to validate the considerably more abstract model from subsection 4.1 in the following section.

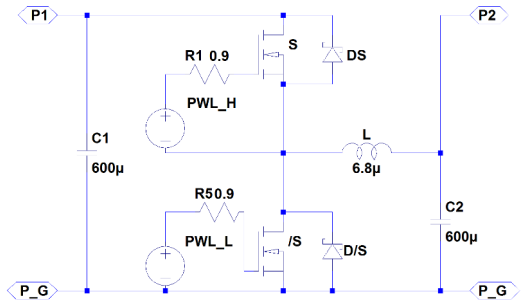

Figure 3. SPICE model of the proposed synchronous half-bridge converter

5 Validation of the proposed model

For parametrization of the models a synchronous half-bridge converter for a typical 48V / 12V conversion has been designed. The converter consists of the MOSFET *IPP052N08N5* (Infineon, 2014), driven by *UCC27210* (Texas Instruments, 2014) the inductance *SER2918H-682* (Coilcraft, 2014) and 60 µF/3 mΩ-capacitors, as well as a Schottky diode *MBR20100CT* (On Semiconductor, 2015) for the SPICE simulation. The values that are required for the parametrization of the model can be taken from the data sheets and are listed in Table 1. The SPICE simulations were carried out with the software *LTSPICE IV* by *Linear Technology*. The simulation environment for the Modelica model is *Dymola* by *Dassault Systèmes*. During the simulations for the validation, the significant speed advantage became apparent. For the computation of an interval of 100 ms the SPICE model takes about 10 min, whereas the Modelica model takes less than 100 ms using an interval length of 10 µs.

Table 1. Model parameters

Name	Value	Description
f_S	200 kHz	Switching frequency
R_{DS}	5.2 mΩ	On-Resistance of the switch
Q_g	42 nC	Total gate charge
$R_{g,total}$	2 Ω	Sum of all gate resistances
V_{drive}	12 V	Gate-drive voltage
L	6.8 µH	Inductance of the inductor
R_L	2.6 mΩ	Resistance of the inductor
$C1, C_2$	60 µF	Capacity of C_1 and C_2
R_{C1}, R_{C2}	3 mΩ	ESR of C_1 and C_2

5.1 Dynamic behavior

In this subsection the dynamic behavior of the proposed model shall be compared with the SPICE model on the basis of step responses on the load current. Therefore, the duty cycle is kept constant and the load resistance is changed to a different load scenario.

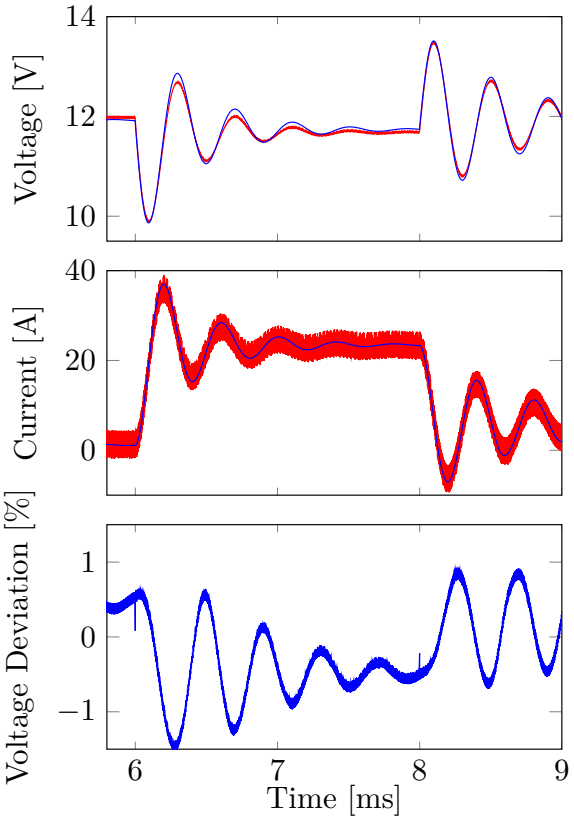

Figure 4. Output voltage and inductor current step response of the Modelica(blue) and the SPICE model(red) to a step in the load resistance during buck mode and the relative voltage deviation between the Modelica to the SPICE model

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The first scenario examines the buck operation. The input v_1 is fed by a constant voltage source of 48 V with an internal resistance of 10 mΩ, the duty cycle is constant at 25 %. In steady state, the load resistance is reduced to 0.5 Ω and after another 2 ms increased to 2 Ω. The result of the simulation is shown in Figure 4. The output voltage and the inductor current are illustrated in the upper two graphs, red for the results of the SPICE simulation, blue for the Modelica model. The lower graph shows the relative error of the output voltage that has a maximum relative error of 1.5 % (absolute 200 mV).

The second scenario examines the boost operation. Now the input is v_2 and is fed by a constant voltage source of 12 V also with an internal resistance of 10 mΩ, the duty is held constant at 25 %. In steady state, the load resistance is reduced to 8 Ω and after another 2 ms increased to 24 Ω. The result of the simulation is shown in Figure 5. The output voltage and the inductor current are illustrated in the upper two graphs, red for the results of the SPICE simulation, blue for the Modelica model. The lower graph shows the relative error of the output voltage that has a maximum relative error of 1.5 % (absolute 720 mV).

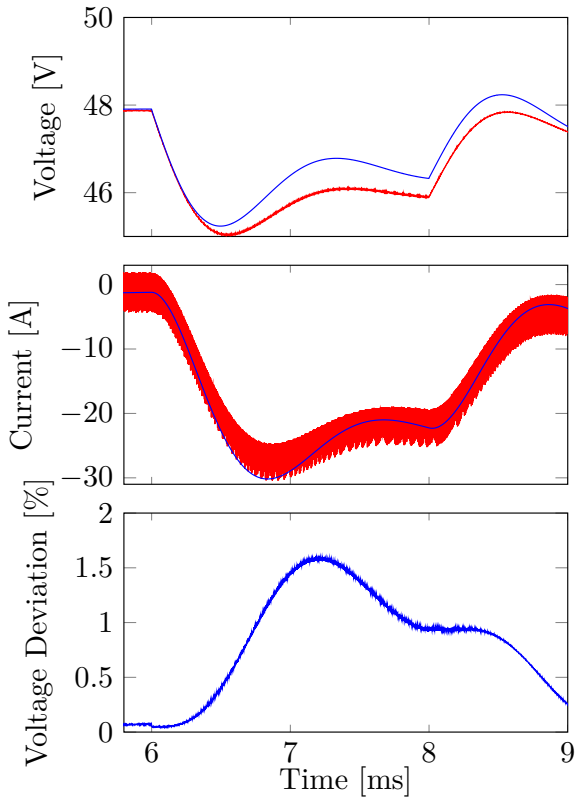

Figure 5. Output voltage and inductor current step response of the Modelica(blue) and the SPICE model(red) to a step in the load resistance during boost mode and the relative voltage deviation between the Modelica to the SPICE model

5.2 Efficiency and losses

In this section, the resulting efficiency of the proposed model shall be compared with the efficiency of the SPICE model. Figure 6 shows the efficiency map of the Modelica model in buck mode as a function of the output current and the duty cycle. The input is fed by a constant voltage source of 48 V.

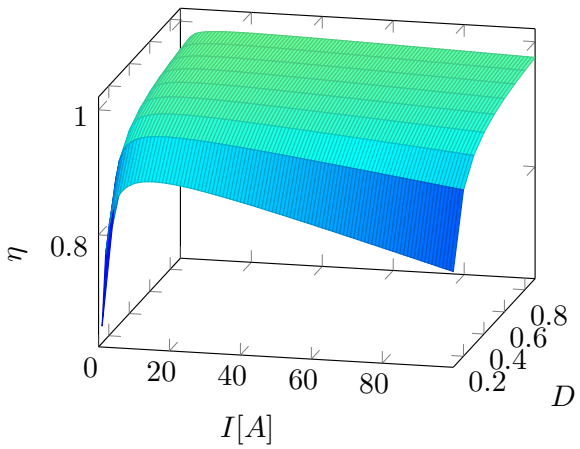

Figure 6. Efficiency map of the proposed Modelica model in buck mode. The input voltage is fixed at 48 V.

The result is the typical efficiency map of a DC/DC converter, having a bad efficiency at low currents, an maximum in the lower quarter of the output current and a subsequent slight lowering of efficiency at higher loads, as there ohmic losses are the dominating effect. Figure 7 shows the absolute deviation

$$\Delta\eta = \eta_{Dymola} - \eta_{SPICE} \tag{16}$$

between the SPICE and the Modelica simulation. It can be seen that in the range of high duty cycles and moderate to high output currents, the absolute deviation is lower than two percentage points. At very low duty cycles there is a trend towards a higher deviation as well as in the area of very low output currents. The negative deviation in the low-current range may be caused by the fact that charging effects of the MOSFET's and diode's parasitic capacitors are not yet implemented in the Modelica model. Reasons for the positive deviation in the range of higher currents are the not yet implemented dead-time losses as well as the effects of ringing in the switching node.

6 Conclusion and Outlook

In the previous considerations, a model of a synchronous half-bridge converter was presented. The model represents losses and the dynamic behavior given by inductors and capacitors of the converter,

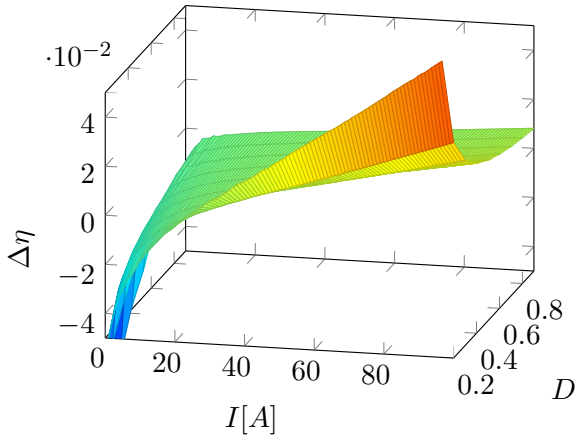

Figure 7. The absolute efficiency deviation $\Delta\eta$ of the SPICE model against the proposed Modelica implementation

without the need of simulating every switching process of the power semiconductors. This approach reduces the calculation effort of the model by several magnitudes. The model can be parametrized easily by using datasheet parameters of the components used in the design. To validate the Modelica model, an equivalent model in SPICE is used which is much closer to physical reality as it takes the switching behavior of the converter into account and uses more detailed semiconductor models provided by the manufacturers. The deviation between both models concerning dynamic behavior during load steps was investigated. It was shown that there is a maximum relative error of 1.5 % in the output voltage of the model in reference to the SPICE model. Furthermore, also the energetic behavior was investigated. It was shown here that the proposed model provides good results for specific operating areas. Still there are some effects which should be considered in future examinations in order improve the accuracy of the model. These are for example losses because of the reverse recovery effect of the diodes or losses due to ripple currents in the capacitors.

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